Notice of Allowability	Application No.	Applicant(s)	
	09/801,564	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/28/2006*.

2. ☒ The allowed claim(s) is/are *1,2,4,5,7-13 and 16-24*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *attached herein* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael L. Drapkin on 06/27/2006.

The application has been amended independent claims 1, 9, and 18 as follows for clarification:

1. (Currently Amended) A processing core, comprising: a first source register including a plurality of first operands, wherein the source address of each first operand is identified in a single instruction; a plurality of second operands, wherein: the plurality of second operands are equal in value to an immediate value, and the immediate value is specified in the single instruction, a prescaler which scales the plurality of operands according to a predetermined scaling factor which is divisable by two; a bitwise inverter coupled to at least one of the first plurality of operands and the prescaled second plurality of operands; a destination register including a plurality of results, a plurality of arithmetic processors respectively coupled to the first operands, prescaled second operands and results, wherein each arithmetic processor computes one of a sum and a difference of the first operand and

a respective prescaled second operand, and wherein the computation operation to be undertaken by each arithmetic processor is specified in the single instruction.

9. (Currently Amended) A method for performing arithmetic processing, the method comprising the steps of: loading a first and second operands from a primary source register; loading a third and fourth operands, wherein: the third and fourth operands are an immediate value specified in an ~~the~~ single instruction, and the third and fourth operands are equal in value; scaling the third and fourth operands according to a predetermined scaling factor which is divisable by two; performing an arithmetic function on the first and scaled third operands to produce a first result; performing the arithmetic function on the second and scaled fourth operands to produce a second result, and storing the first and second results in a destination register.

18. (Currently Amended) A method for performing arithmetic processing, comprising the steps of: receiving a single instruction comprising an arithmetic function to be performed using an immediate value, and operands from first and second source addresses in a primary source register, wherein the immediate value and the first and second source addresses are specified in the single instruction; loading a first and second operands respectively from the first and second addresses in the primary source register, loading a third and fourth operand each comprising the immediate value; scaling the third and the fourth operand according to a predetermined scaling factor which is divisable by two; performing the arithmetic function on the first operand and the scaled third operand to

produce a first result; performing the arithmetic function on the second operand and the scaled fourth operand to produce a second result; and storing the first and second results in a destination register.

REASONS FOR ALLOWANCE

2. Claims 3, 6, and 14-15 are cancelled.

3. Claims 1-2, 4-5, 7-13, and 16-24 are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a method for performing an arithmetic processing comprising: loading first, second, third, and fourth operands wherein the third and fourth operands are equal to immediate value specified in an instruction; scaling the third and fourth operands with a factor divisable by 2; performing arithmetic on the first with third operands and the second with fourth operands to yield a first and second results respectively; store the results in a register as seen in independent claims 1, 9, and 18.

The closest found prior arts are Lin et al. (U.S. 5,959,874), Nakakimura et al. (U.S. 5,915,109), and Phillips Inc. ("An Introduction to Very-Long Instruction Word (VLIW) Computer Architecture"). Lin et al. in view of Nakakimura et al. and in further view of Phillips disclose a method for performing an arithmetic processing comprising: loading first, second, third, and fourth operands and performing arithmetic on the first

with third operands and the second with fourth operands to yield a first and second results respectively and store the results in a register. However, Lin et al. in view of Nakakimura et al. and in further view of Phillips fail to disclose a step of scaling the third and fourth operands with a factor divisable by 2 prior arithmetic operation as seen above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on 7:00AM to 5:00PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C Do
Examiner
Art Unit 2193

June 29, 2006

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